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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,454	11/26/2003	Jacek Budny	10559-874001 / P17393	5960

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EXAMINER	
ALROBAYE, IDRISS N	
ART UNIT	**PAPER NUMBER**
2183	
MAIL DATE	**DELIVERY MODE**
06/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/723,454	**Applicant(s)** BUDNY ET AL.	
	Examiner Idriss N. Alrobaye	**Art Unit** 2183	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 22 May 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the sa me day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expire _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid d ismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejec ted claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL -324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *1-39*.

   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final actio n, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☒ Other: see Continuation Sheet.

Continuation of box 13

1. As per claim 1,

2. **Applicant's argument 1:**

"Applicant's independent claim 1 recites "[a] method of co-processing, comprising: connecting an interface of a first processor to an interface of a second processor using a bus, the interface of the second processor being configurable to place the second processor in a slave processing mode or a master processing mode."
In contrast, Sexton does not describe these features. Rather, Sexton describes programmable logic controller that includes a function block processor 110 for processing function block instructions and a bit processor 120 for processing Boolean instructions (FIG. 2, Abstract, and col. 2, lines 36-59). Both the block processor 110 and the bit processor 120 are incorporated into the same single controller module (see FIG. 2, and col. 4, lines 38-42.)"

3. **Examiner's Response:**

The programmable logic controller taught by Sexton is considered equivalent to the co-processing in claim 1. Further, it implies from the applicant's argument that the first processor and the second processor are in separate controller modules. It is noted that the features upon which applicant relies (i.e., first processor and the second processor on a separate controller module) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, it is irrelevant whether the block processor 110 and bit processor 120 are incorporated into the same controller module. All the features recited in claim 1 are shown by the reference Sexton, for instance, co-processing (see Sexton, col. 1, lines 48-67), an interface of a first processor and interface of second processor is also

shown by Sexton, see col. 1, lines 48-67, wherein a two processor architecture is employed. The two processors architectures are equivalent to the first and second processor. Also, in col. 1, lines 48-67, it uses a very similar language as in claim 1, "processor-coprocessor programmable logic controller" which is considered equivalent to the co-processing in claim 1. The Input/output of the two processors are considered equivalent to the interface.

For more about the functionality of two processors shown by Sexton see the detailed explanation of the claim rejections in the Final Action sent on 04/24/2007.

4. Applicant's argument 2:

Thus, it is the bit processor 120 that places itself in master mode or in slave mode. Sexton does not describe that an interface of the bit processor 120 or of function block 110 causes the bit processor 120 to be placed in master or slave mode. Indeed, because the function block processor 110 and bit processor 120 are included in the same physical module (namely, the logic controller) and were thus designed to work in tandem, there is no need whatsoever for an interface to facilitate inter-operability between processors not specifically designed to work in tandem and configured to place a processor in master or slave mode, Accordingly, Sexton fails to disclose or suggest at least the feature of "connecting an interface of a first processor to an interface of a second processor using a bus, the interface of the second processor being configurable to place the second processor in a slave processing mode or a master processing mode," as required by applicant's independent claim 1. Applicant's independent claim 1, and the claims that depend from it are therefore patentable over the cited art.

5. Examiner's Response:

The current language of claim 1 recites "sending a task from the first processor to the second processor through the bus, the task comprises an instruction that places the

second processor in a salve processing mode". The reference, Sexton shows this limitation, see col. 5, lines 47-67, wherein the start command is the instruction.

As for the first limitation of claim 1, it recites, "connecting an interface of a first processor to an interface of a second processor using a bus (see Sexton, Fig. 1, wherein the output of the first processor (element 110) is considered equivalent to an interface of the first processor and the input of the second processor (element 120) is considered equivalent to an interface of the second processor. Thus, the output (interface) of element 110 is connected to the input (interface) of element 120 using a bus).

The second part of the first limitation of claim 1 recites "the interface of the second processor being configurable to place the second processor in a slave processing mode or a master processing mode". As the command sent from the first processor (element 110), it passes through the input of the second processor (element 120) and thus places the processor in either a slave processing mode or master processing mode. Thus, without the input of the second processor (element 120), the second processor would not be able to function as a slave or a master processor.

Therefore, the argued claims stand as previously rejected.

Suggestions: The examiner suggests to the applicant to focus on Fig. 4, and specifically to the structure of the components in the figure. Focusing on Fig. 4 may possibly overcome the used reference.

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